An EM-aware methodology for a high-speed multi-protocol 28Gbps SerDes design with TSMC 16FFC

Helic / Wipro / NXP

ABSTRACT

With data rates pushing past 10Gbps and up to 56Gbps, SerDes design has become increasingly challenging. To achieve demanding performance requirements driven by the protocol specifications, it is common for designers to use on-chip inductors to implement filtering techniques in the transmitter and receiver data lanes as well as low noise LC-tank oscillators for PLL lanes. The increase of internal clock frequencies and data rates requires that Electromagnetic (EM) phenomena, like parasitic inductance and magnetic coupling, can no longer be ignored in such designs. The faster the data rate/clock speed, the more difficult it is to predict and manage unwanted behaviour due to such phenomena. In order to overcome these design challenges there is a need for a new design methodology which includes an EM modeling engine that has the following key features:

(i) Very high capacity with no compromise in accuracy

(ii) Very fast extraction times (comparable to RC parasitic extraction engines)

(iii) Tight integration into the Custom IC design flow. I.e. seamless interface with both front-end (layout, schematic editors) and back-end (LVS/RCX) tools

Traditional EM solvers fall far short of the requirements stated above. They are typically unable to deal with the high complexity and dense metallization of an analog and mixed-signal design like a 28Gbps SerDes. Having been designed primarily to model passive spiral structures with a few ports (typically less than 10), the size and complexity of the metallization that needs to be extracted in these designs easily overwhelms the capacity of traditional EM tools. Massive networks of interconnects, ground networks and power grids comprising of hundreds of ports are totally out of their scope.

The Wipro design team recently developed and tested silicon for a 28Gbps SerDes system for NXP that features simultaneous multi-lane and multi-protocol support. The SerDes IP is implemented with TSMC's 16nm FINFET process which helps to control costs and power for high-performance designs. This system integrates 8 data lanes and 2 PLL lanes containing 4 LC voltage controlled oscillators (LC-VCOs) that support data rates from 28G to 16G, 10G, 5G and below. Various Helic generated and modeled structures are implemented in the data and PLL lanes as well as the global clock distribution network.

In this presentation, Helic and Wipro's High-Speed SerDes Analog & Mixed-signal Design Team describe their collaboration and a design methodology that has resulted in three generations of first-pass success SerDes IP families for NXP (using IBM/FSL 45nm-SOI and TSMC's 28nm and 16nm process nodes). Wipro employs Helic's VeloceRF and RaptorX software comprising a complete EM-aware design methodology that starts from optimal, DRC-clean spiral device synthesis and floor-planning, introduces EM-extraction in-the-loop and closes the flow with EM-signoff post-LVS. Helic's tools are being used in the flow to capture electromagnetic coupling effects between spiral passives, interconnects, power and signal lines and the power grid, from the earliest design stages leading to compact circuit sizes and notably shorter design cycles. The tight integration of Helic's software suite in TSMC 16nm PDKs and Cadence Custom IC design flow improves productivity and data management. These benefits enable Wipro's team to meet accelerated time-to-market challenges with no performance compromise.

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Bud Hunter, SerDes Analog IC Design Manager, Wipro
Kelly Damalou, Sr. Technical Account Manager, Helic

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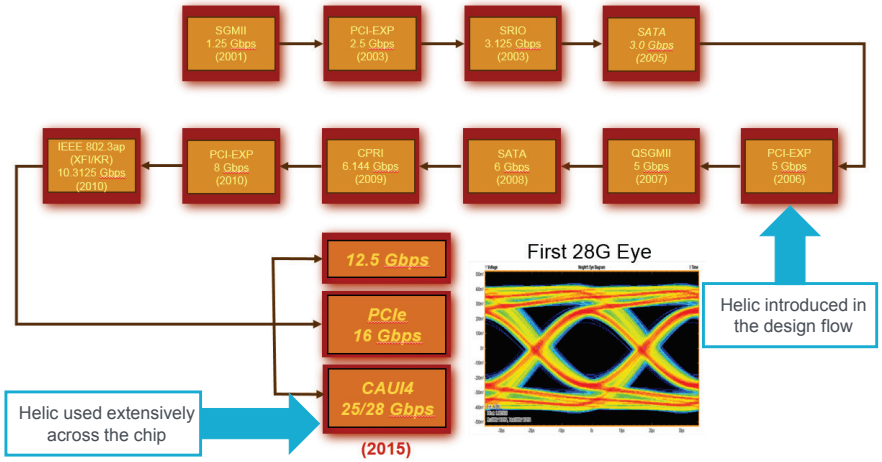
Agenda

- The SerDes design: Description and Challenges
- Design methodology
- Metrics and silicon results
- Helic methodology benefits
- Conclusion

Wipro/NXP SerDes IP History with Helic

- Wipro High-Speed SerDes Analog & Mixed-signal Design Team develops IP for the NXP Digital Networking business unit
- Longstanding relationship with Helic
- Continuous improvements to the Helic tool suite
- Multiple generations of successful first-pass SerDes IP families for NXP:
  - 10G SerDes – 28nm TSMC
  - 28G SerDes – 16nm FinFET TSMC
- Silicon-proven 28Gbps SerDes system with simultaneous multi-lane and multi-protocol support:
  - IP integrates 8 data lanes and 2 PLL lanes containing 4 LC voltage controlled oscillators (LC-VCOs) that support data rates from 28G to 16G, 10G, 5G and below
  - Implemented with TSMC's 16nm FinFet process

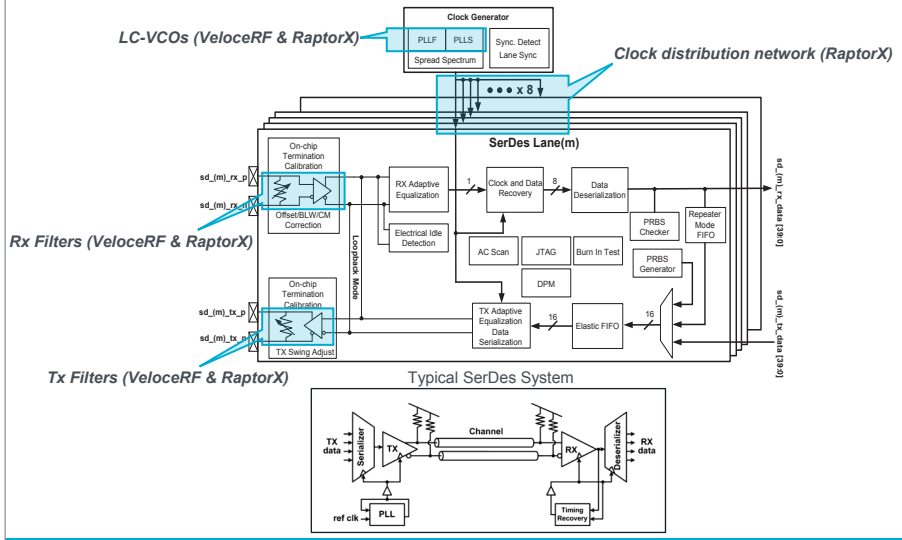
Wipro/NXP SerDes IP History with Helic



EM challenges in Wipro/NXP 28Gbps SerDes IP

- SerDes design at data rates as high as 28G requires highly accurate and efficient electromagnetic modeling for:
  - Differential inductors and Tcoils
  - Global clock distribution networks
- Wipro integrated 15 inductive structures that required accurate EM modeling:
  - 4 LC-VCO inductors
  - 2 Transmitter Tcoils for bandwidth extension and return loss
  - 6 Receiver inductors for gain stages in the high speed path
  - 1 Receiver inductor placed under a bump for input return loss
  - 1 Receiver Tcoil for output buffer bandwidth extension
  - A 4800µm global clock distribution network

Wipro/NXP 28Gbps SerDes Design Case



Why Helic?

- DRC-clean pCells with dummy fill
- High-capacity EM engine
- Optimization of silicon real-estate
- Seamless flow integration in Cadence and NXP design flow
- Competitive extraction and simulation times

Helic Products in the SerDes Design Flow

VeloceRF Advanced

ANALOG IP/DEVICE SYNTHESIS

Inductor, transformer and t-line synthesis & modeling tool.

Instantiates ready-to-tape-out layouts and provides highly accurate SPICE models, silicon verified up to110GHz.

Analog IP compiler platform

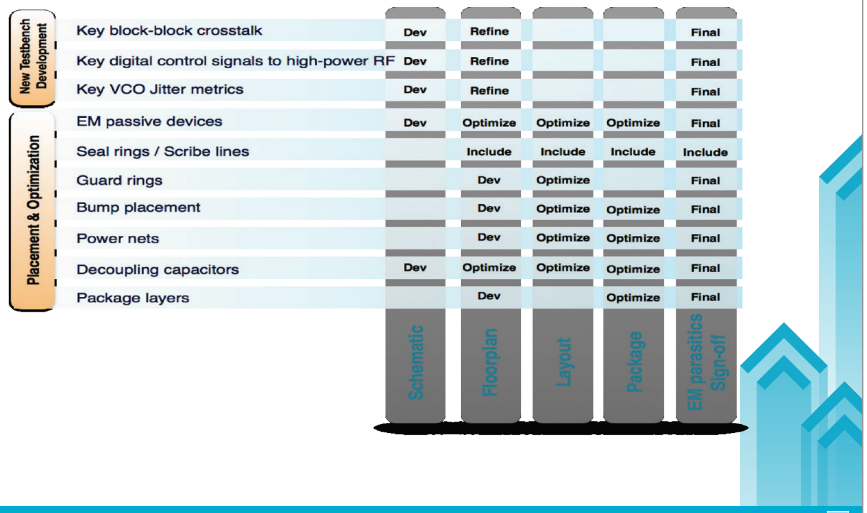
RaptorX Advanced

EM MODELING

Novel electro-magnetic modeling software, pre-LVS back-annotation of model to Schematic.

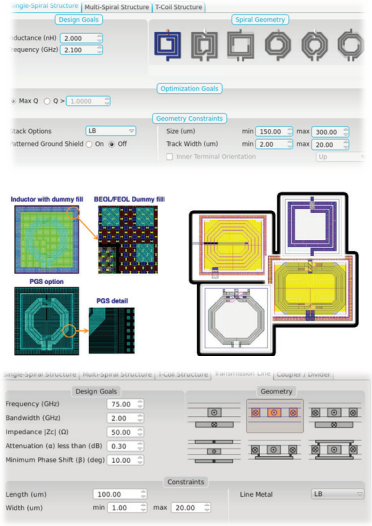
High capacity engine combined with highly accurate results and blazing fast modeling times are the core differentiating factors

Helic EM Methodology



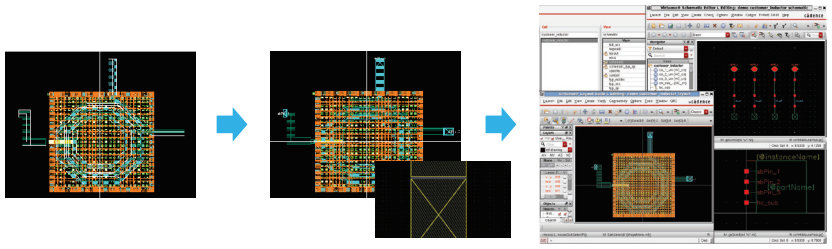
Design Efficiency with VeloceRF

- **Fast, Flexible** Inductor Design Capability
- **Rich** inductor/transformer pCell library
- **Fully integrated** to common design platforms/tools
  - Supports ICADV12.2
  - Fully compatible with LVS (Assura, PVS, Calibre, ICV) & Extraction (QRC, CalibreXRC, StarRC etc.) tools
- **Silicon Accurate**
  - Hundreds of production tapeouts in all geometries (down to 16nm)
  - In-house silicon characterization lab



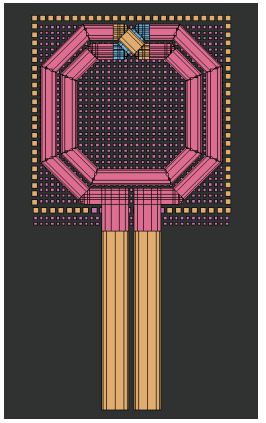
RaptorX Custom Device flow

- Enables physical verification for custom passives, proprietary/legacy cells, arbitrary structures
- Supports any 3rd party LPE flow
- For each Custom Device:
  - Recognition layers are automatically added
  - Layout, Schematic, Symbol and model views are saved in the design database



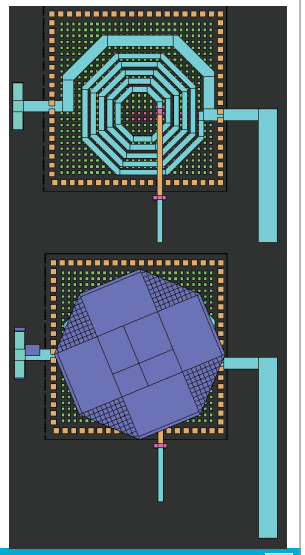
SerDes LC-VCO Methodology

- **Magic Wand** synthesis engine delivers inductor pCells for the four LC-VCOs based on user defined design constraints
- **Helic pCell properties** can be changed on the fly and quickly analyzed.
- **Benefits** for the LC-VCO designs:
- Improves initial concept development: multiple inductor analyzed and modified at once
- Saves significant amount of time vs. traditional iterative layout & extraction methods
- Improves efficiency of initial floorplanning and changes that impact the area footprint



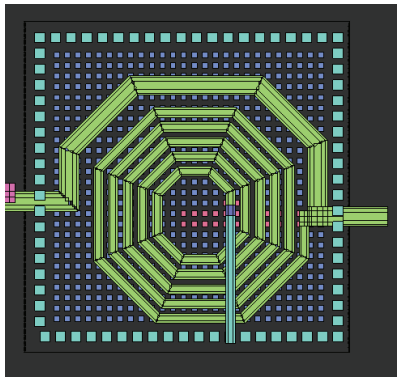
SerDes Receiver Methodology

- **VeloceRF Magic Wand** synthesis engine generates receiver high speed gain stage inductors.
- Inductors are customized and modeled using **RaptorX Custom Device** feature.
- Input return loss inductor is a special case due to being placed directly under the bump for area savings.
  - Placing an inductor under a bump can have significant impact on its performance.
  - Separate RaptorX Custom Device is modeled with the bump included to accurately capture the effects of the bump.



SerDes Transmitter Methodology

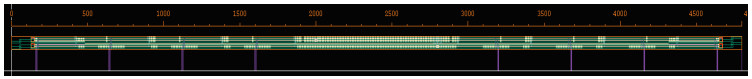
- Transmitter bandwidth extension and return loss Tcoils are
  1. Generated with VeloceRF
  2. Converted to RaptorX Custom Devices
- Additional effects from routing leads of Tcoils to the output driver are captured
  - Relatively short metal routes can add a significant amount of inductance to the Tcoils and impact the Transmitter performance



Routing leads could account for ~10% of the coil inductance

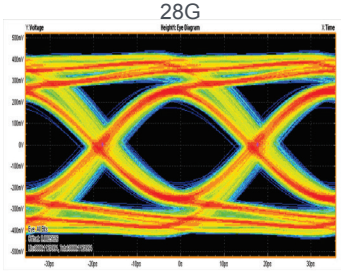
SerDes Global Clock Network Methodology

- The global clock distribution is a fully EM modeled with RaptorX Custom Device feature (> 4.5mm long).
- The transmission line delivers clock to the entire SerDes system up to 28GHz frequencies and must be modeled accurately.
- Traditional methods involve manually adding parasitic effects into an RC netlist which is prone to error and could result in performance failures or overdesign with respect to area and power.

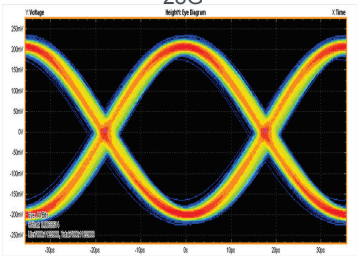


Silicon results: Transmitter Eye Diagrams

28G

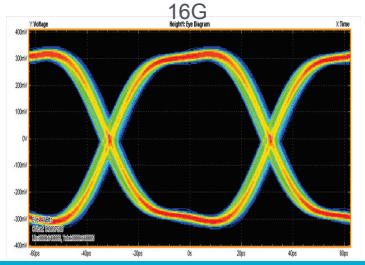


28G

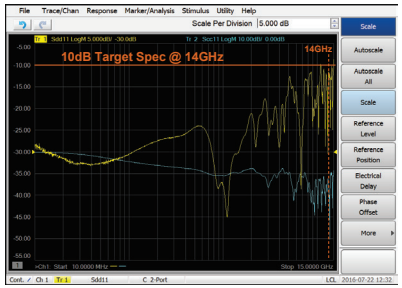


25G

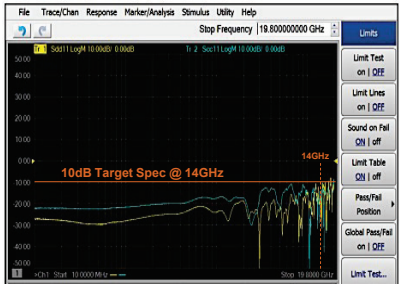
16G



Silicon results: Transmitter and Receiver Differential Return Loss



TX DRL



RX DRL

- 10dB DRL targets achieved in the 8-14GHz range in order to meet the 16G & 28G 6dB protocol specs

Helic methodology benefits

- Captures all electromagnetic effects (coupling & crosstalk)
  - Models guard rings, dummy fill, custom routing, bump pads
- Efficient floorplanning
  - Reduces silicon real-estate
- Shorter design cycle
- First-pass silicon
  - No test vehicle chips required
  - Saves thousands of $

Model Everything